Notice of Allowability	Application No.	Applicant(s)	
	09/708,490	IWASA, CHIE	
	Examiner	Art Unit	
	Tung S Lau	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *5-24-2004*.

2. ☒ The allowed claim(s) is/are *1-19*.

3. ☒ The drawings filed on *06 January 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. ROTELLA, ROBERT on June 28, 2004.

The application has been amended as follows:

Replace claim 1 with:

1. (Currently Amended) A semiconductor testing apparatus for testing semiconductor devices, ~~configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacturer as faulty samples so as to improve testing performance, the semiconductor testing apparatus~~ comprising:

an IDDQ measuring circuit configured to measure current data of good samples and ~~the~~ samples returned by ~~the~~ a user, by supplying test vector data to the good and returned samples;

a determination circuit configured to determine a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices based upon the measured current data,

wherein the IDDQ measuring circuit tests the target semiconductor devices by applying the test vector data for the effective address pairs, and

wherein the semiconductor testing apparatus is configured to feed back data of the returned samples which have been shipped as the good samples, but returned from the user to a manufacturer as faulty samples so as to improve testing performance.

Replace claim 5 with:

5. (Currently Amended) A semiconductor testing method for testing semiconductor devices, ~~configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacturer as faulty samples so as to improve testing performance, the method~~ comprising:

reading test vector data;

measuring current data of good samples and ~~the~~ samples returned by ~~the~~ a user, by supplying the test vector data to the good and returned samples;

determining a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices based upon the measured current data; and

applying the test vector data for the effective address pairs to the target semiconductor devices for testing,

wherein the semiconductor testing method is configured to feed back data of the returned samples which have been shipped as the good samples, but

returned from the user to a manufacturer as faulty samples so as to improve testing performance.

Replace claim 9 with:

9. (Currently Amended) A program with which a semiconductor testing method is executed by a computer in a semiconductor testing apparatus which comprises a read circuit, a determination circuit, and an IDDQ measuring circuit configured to test semiconductor devices by applying test vector data, ~~configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacturer as faulty samples so as to improve testing performance,~~ the program comprising:

instructions configured to read the test vector data;

instructions configured to supply the test vector data to good samples and ~~the~~ samples returned by ~~the~~ a user;

instructions configured to measure current data of the good and returned samples;

instructions configured to determine a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices based upon the measured current data; and

instructions configured to apply the test vector data for the effective address pairs for testing.

wherein a semiconductor testing apparatus is configured to feed back data of the returned samples which have been shipped as the good samples, but returned from the user to a manufacturer as faulty samples so as to improve testing performance.

Replace claim 13 with:

13. (Currently Amended) A semiconductor testing method of specifying a faulty part in a semiconductor device, ~~configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacturer as faulty samples so as to improve testing performance,~~ the method comprising:

reading a test program and test vector data;

supplying the test vector data to good samples and ~~the~~ samples returned by ~~the~~ a user;

measuring current data of the good samples and returned samples, employing an IDDQ measuring circuit;

determining a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices in a manufacturing process based upon the measured current data;

applying the test vector data for the effective address pairs to a target semiconductor device; and

specifying a faulty part within the target semiconductor device by measuring an emission from the target semiconductor device,

wherein the semiconductor device is configured to feed back data of the returned samples which have been shipped as the good samples, but returned from the user to manufacturer as faulty samples so as to improve testing performance.

Replace claim 16 with:

16. (Currently Amended) A semiconductor testing apparatus for specifying a faulty part in a semiconductor device, ~~configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacturer as faulty samples so as to improve testing performance,~~ the apparatus comprising:

a read circuit configured to read test vector data and a test program;

an IDDQ measuring circuit configured to measure current data of good samples and ~~the~~ samples returned by ~~the~~ a user, by supplying the test vector data to the good and returned samples;

a determination circuit configured to determine a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices in a manufacturing process; and

a faulty part specifying circuit configured to apply the test vector data for the effective address pairs to the target semiconductor device and to specify a faulty part by measuring an emission from the target semiconductor device,

wherein the semiconductor testing apparatus is configured to feed back data of the returned samples which have been shipped as the good samples, but returned from the user to a manufacturer as faulty samples so as to improve testing performance.

Replace claim 19 with:

19. (Currently Amended) A program with which a semiconductor testing method is executed by a computer in a semiconductor testing apparatus which comprises a read circuit, a determination circuit, and a faulty part specifying circuit, ~~configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacturer as faulty samples so as to improve testing performance,~~ the program comprising:

instructions configured to read a test program and test vector data;

instructions configured to measure current data of good samples and ~~the~~ samples returned by ~~the~~ a user, employing an IDDQ measuring circuit, by supplying the test vector data to the good and returned samples;

instructions configured to determine a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices in a manufacturing process based upon the measured data;

instructions to apply the test vector data for the effective address pairs to the target semiconductor device; and

instructions to specify a faulty part within the target semiconductor device by measuring an emission from the target semiconductor device,

wherein the semiconductor testing apparatus is configured to feed back data of the returned samples which have been shipped as the good samples, but returned from the user to a manufacturer as faulty samples so as to improve testing performance.

Amendments to claims 1, 5, 9, 13, 16, 19 were made to define over the applied prior art. This system is deemed to be non-obvious over the systems of the prior art.

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung S Lau whose telephone number is 571-272-2274. The examiner can normally be reached on M-F 9-5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 571-272-2269. The fax phone numbers for the organization where this application or proceeding is assigned is 703-872-9306

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TL

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